$L_2min^{2/2s}$: Efficient Linear Reconstruction Filter for Incremental Delta-Sigma ADCs

Bo Wang, *Senior Member, IEEE*, Man-Kay Law, *Senior Member, IEEE*, and Jens Schneider, *Member, IEEE*

***Abstract*—While it becomes more challenging to improve the energy efficiency of incremental delta-sigma data converters (IDCs) from the analog circuit design perspective, we propose two novel linear reconstruction filters for IDCs to enhance their performance in a digital way, including the L_2min^2 filter and its symmetric version, the L_2min^{2s} filter. Compared to the classical linear reconstruction filters, such as the cascade-of-integrators (CoI) and cascaded integrator-comb (CIC) filter (an implementation of *sinc* filter), the proposed filters can achieve efficient quantization and thermal noise suppression, with the lowest thermal noise penalty factor of 1.2 among the high-order linear reconstruction filters. In this paper, we present analytical, numerical, and experimental results to demonstrate the superior performance of the filters for first-order and second-order IDC output reconstruction. The proposed filters are hardware-friendly and example digital implementations in a standard complementary metal-oxide-semiconductor (CMOS) and field-programmable gate array (FPGA) platforms are included in this paper.**

***Index Terms*—Analog-to-digital data converter, incremental delta-sigma ADC, reconstruction filter, digital linear filter, thermal noise penalty, L_2min^2, L_2min^{2s}, frequency notch.**

I. Introduction

EMPOWERING various industries, such as telecommunication, healthcare, automotive, etc., analog-to-digital converters (ADCs) have played a crucial role in bridging the gap between the physical world and the digital realm [1], enabling the processing, storage, and manipulation of real-world data digitally. Recent advances, such as sensor fusion, have raised high demands for data and, consequently, high-performance ADCs. In pursuit of this goal, various new quantization schemes have been reported. The recent pioneers in this field include unlimited sampling [2], [3] and one-bit quantization [3], [4], [5], [6], [7], [8], [9], which utilize advanced signal processing theories and powerful signal processing tools for signal recovery. However, substantial computational resources are required (e.g., 0.3 ms computation time in a typical CPU [9]). Among the classical quantization schemes, delta-sigma ($\Delta\Sigma$) ADC also relies on signal processing to reconstruct the input using the quantized one-bit or multi-bit output [1], [10]. However, its signal reconstruction process is more hardware-friendly to be integrated into standalone ADC chips. Meanwhile, compared to the emerging one-bit quantization scheme using time-varying thresholds drawn from a predefined distribution [3], [4], [5], [6], [7], [8], [9], the loop filter in a $\Delta\Sigma$ ADC can effectively generate uniform distancing time-varying thresholds, which recursively makes the threshold closer to the input signal, thus accurate signal recovery becomes possible using simple digital processing.

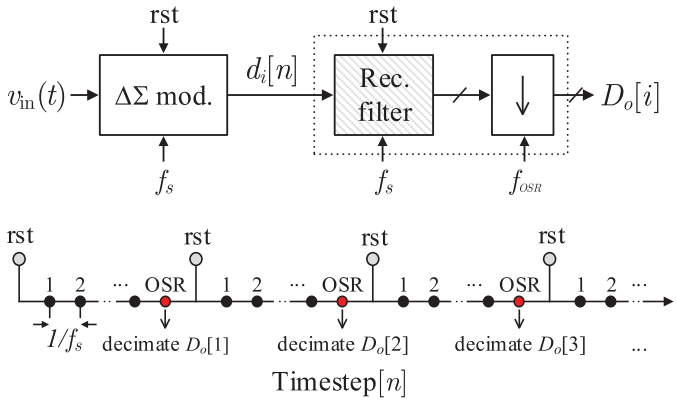

Fig. 1. A typical IDC and its system operation [12], [13]. $v_{\rm in}(t)$: input signal; f_s: modulator sampling rate; i: A/D sample index; n: discrete timestep; $D_o[i]$: $i^{\rm th}$ decimated A/D digital output.

One $\Delta\Sigma$ ADC variant is called incremental $\Delta\Sigma$ ADC (IDC), which is popular for applications requiring sample-to-sample conversion, i.e., Nyquist-rate conversion [11]. As shown in Fig. 1, a typical IDC consists of a $\Delta\Sigma$ modulator, a reconstruction filter, and a decimation operation [12], [13]. Its working principle is similar to the conventional free-running $\Delta\Sigma$ ADC. The main difference is the extra modulator and reconstruction filter reset operation after every OSR cycle (i.e., oversampling ratio) to eliminate any memory effect. This unique feature allows IDC to perform sample-to-sample conversion, akin to a Nyquist-rate converter, while also benefiting from the oversampling and quantization noise-shaping capabilities of a free-running $\Delta\Sigma$ ADC [1].

To improve the IDC performance, such as achieving higher resolution with lower energy consumption, prior research has

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primarily focused on optimizing the $\Delta\Sigma$ modulator. This includes utilizing new analog integrator topologies to reduce system power [14], employing multi-step conversion for greater quantization noise suppression [15], [16], [17], utilizing time-domain quantizers to leverage the process scaling benefits [18], etc. However, the reconstruction filter has not received the same level of attention. This is why statements such as "*a one-bit first-order modulator requires 2^k samples to achieve k-bit resolution*" occasionally appear in the literature, which is false if a digital filter other than a simple counter is used to process the modulator output [11]. For instance, for a one-bit first-order modulator in Fig. 2, achieving 10-bit resolution would require 1024 samples if a counter is used for input reconstruction. However, by adopting an optimal reconstruction filter [19], only 98 samples are needed to achieve the same mean squared error (MSE) equivalent to 10-bit resolution [12]. Therefore, designing effective reconstruction filters is an alternative way to improve IDC performance deserves more research focus.

A. Prior Art of IDC Reconstruction Filter

There are two categories of IDC reconstruction filters: linear ones and nonlinear algorithmic ones. When evaluating these filters, three metrics are primarily considered: quantization noise suppression, random noise suppression, and hardware complexity. Below is a brief overview of the existing reconstruction filters with their performance discussed based on these evaluation metrics.

The first class comprises linear ones, such as the widely used cascade-of-integrators (CoI) filter and *sinc* filter operating in transient mode [20], i.e., with periodic reset. Although these filters have appealing implementation simplicity, they cannot fully utilize the information encoded in the $\Delta\Sigma$ modulator output. As a result, compared to an ideal filter, they suffer from signal-to-quantization-noise ratio (SQNR) losses ranging from a few to a few tens of decibels after reconstruction [12]. A recently modified CoI filter [21] performs slightly better by incorporating a lossy digital integrator stage. However, its on-chip implementation is costly due to the requirement of fixed-point multiplication operations. Increasing the order of CoI or *sinc* filter can enhance quantization noise suppression but leads to a degradation in their ability to suppress random noise, such as thermal noise [11]. Therefore, it becomes challenging for CoI and *sinc* filter to achieve effective quantization and thermal noise suppression simultaneously. Steensgard et al. [22] derive an SNR-optimized IDC reconstruction filter, which ended up with irregular filter weights, making it challenging to implement on-chip.

The second class comprises nonlinear algorithmic ones, such as the optimal filter [19], surrogate constraint algorithm [23], dynamic rational cycle decoding [24], direction projection algorithm [25], recursive filter [26], block-based decoder [27], etc. Although good quantization noise suppression can be achieved, they are all algorithmic without straightforward hardware implementations. Additionally, their high memory and computational overhead render them unpopular in actual IDC design, which prefers employing simple digital logic to build the output filter on-chip [28]. Furthermore, these algorithmic filters' random noise suppression capabilities are still questionable. For instance, Kavusi et al.'s optimal filter [19] cannot process modulator output with random noise present. Server-side signal reconstruction approaches, such as phase retrieval [5], covariance recovery [6], etc., can also be potentially applied to IDCs. This paper mainly focuses on linear reconstruction filters that can be implemented on standalone ADC chips, and a full review of the literature on server-side signal reconstruction is out of the scope of this work. Instead, we would like to refer the readers to, e.g., [2], [6] and the references therein for their operation principles.

B. Technical Contributions and Results Overview

This paper proposes two novel linear digital filters for IDC output reconstruction. Compared to the prior arts, the proposed filters can achieve **efficient quantization and thermal noise suppression** simultaneously and are **hardware-friendly to be implemented in ADC chips**. Specifically,

1. **theory-wise,** we optimized an L_2-norm function to minimize the output reconstruction error of a first-order IDC, resulting in a new filter kernel L_2min^2. Besides its high quantization noise suppression capability, its thermal noise penalty factor is only 1.2 (see Section III-C), the lowest among all existing high-order ($\geqslant 2$) linear filters. In this paper, we further utilize this filter kernel to build a symmetric filter L_2min^{2s} that can achieve periodic noise suppression (e.g., power line noise). The analysis and numerical results show that our proposed filters can perform better than the popular CoI and *sinc* filters, especially for thermal-noise-limited first-order and second-order IDC output reconstruction. For instance, to achieve the same thermal noise level, using the proposed filter can reduce the IDC energy consumption by 11%, 28%, and 33% compared to that of using a CoI^2/$sinc^2$, $sinc^3$, and CoI^3 filter, respectively. All numerical simulation and implementation scripts of our proposed filters are open-source[1];
2. **hardware-wise,** we present a full-custom digital design to implement the proposed filter kernels, with bit-truncation applied to minimize their digital overhead. We also present synthesis implementations for FPGA and ASIC targets. The performance of the proposed reconstruction filter is also experimentally verified using the output of a second-order IDC silicon chip prototype [29].

C. Organization and Notations

Section II revisits the generic first-order IDC operation. We then present the derivation, analysis, and verification of the proposed L_2min^2 filter and its symmetric version, the L_2min^{2s} filter, in Section III and IV, respectively. This is followed by an example design using the proposed filters in Section V. Their digital implementations are detailed in Section VI, with a performance summary in Section VII and a conclusion in Section VIII.

[1]download from github.com/bowanghbku/L2min2-Filter

Notation: Throughout this paper, we use n to denote the discrete sample timestep at a sampling frequency of f_s; N is the total number of samples used in one conversion (i.e., OSR). $d[n]$ is the quantized modulator digital output at timestep n, with a quantization error $\varepsilon[n]$. σ_ε denotes the standard deviation of $\{\varepsilon[n], n = 1, \ldots, N\}$, and σ_q is the ADC quantization noise. s_n represents $\sum_{i=0}^{n-1} d[i]$. w_n is the filter weight of $d[n]$ when used to produce a reconstructed input $\widehat{v}_{\text{in}}$, with the true input v_{in}. The peak-to-peak resolution of the ADC is denoted as k or k-bit, with $U_{\max}$ representing the ADC's maximum stable input range. l is the number of quantization levels of the modulator. L represents the order of a *sinc*^{L} filter with D denoting its decimation ratio. $(2M-1)$ denotes the kernel length of an $L_2\text{min}^{2s}$ filter. In numerical computations, $\lceil\cdot\rceil$ is the ceiling function.

II. The Basic Operation of IDC

In this section, we lay the basis for deriving our proposed filter by reviewing the time-domain operation of a first-order incremental $\Delta\Sigma$ modulator. Note that time-domain instead of frequency-domain analysis is usually preferred for IDCs [11]. Fig. 2 shows a generic bipolar modulator using a one-bit quantizer. Assuming the input $v_{\text{in}} \in [-1, 1]$ is constant within one conversion [13], with the comparison threshold of its quantizer being 0 and the output $d[n] \in \{-1, 1\}$. The integrator is reset at the beginning of each conversion (i.e., $u_1[0] = 0$). Particularly, $d[0] = 0$ is used to avoid the feedback operation during the first integration cycle [30]. For a discrete-time integrator (the conclusion of this paper also holds for continuous-time ones), its output $u_1[n]$ at the n^{th} clock cycle is

$$u_1[n] = u_1[n-1] + v_{\text{in}} - d[n-1], \quad n \geqslant 1 \tag{1}$$

After simplifying this recursive relationship,

$$u_1[n] = n \cdot v_{\text{in}} - \sum_{i=0}^{n-1} d[i] \overset{\text{def}}{=} n \cdot v_{\text{in}} - s_n, \quad n \geqslant 1 \tag{2}$$

where s_n is the running sum of $d[0]$ to $d[n-1]$. Eqn. (2) holds for $n \in [1, N]$, with $s_n \in [-n+1, n-1]$ and $s_n \in \mathbb{Z}$. Because the quantizer compares $u_1[n]$ with 0, the digital output of the modulator is

$$d[n] = \begin{cases} +1 & n \cdot v_{\text{in}} \geqslant s_n, \\ -1 & n \cdot v_{\text{in}} < s_n, \end{cases} \quad n \geqslant 1 \tag{3}$$

The encoded output $d[n]$ for any v_{in} can be derived following (2) and (3). For example, with $v_{\text{in}} = 0.437$, Fig. 3(a) shows the relative values of $n \cdot v_{\text{in}}$ and s_n at different cycles. As depicted in Fig. 3(b), the sequence s_{n+1} (not s_n due to a delay) forms an envelope to closely track the input ramp $n \cdot v_{\text{in}}$ [12]. The tracking error $\varepsilon[n] = s_{n+1} - n \cdot v_{\text{in}}$ in each cycle is plotted in Fig. 3(c), with $\lim_{N\to\infty} \sum_{n=1}^{N} \varepsilon[n]/N = 0$.

A digital reconstruction filter then estimates the input by computing the inner (dot) product between the modulator output $d[n]$ and the filter's fixed-width weighting function w_n, that is $\sum_{n=1}^{N} (d[n] \cdot w_n) \,/\, \sum_{n=1}^{N} w_n$. As the $\Delta\Sigma$ modulator is nonlinear, its quantization error varies with the input. A filter that can minimize both the peak quantization error and the overall MSE (i.e., average accuracy [31]) across the whole input range is often preferred. Currently, the most popular filters for IDC output reconstruction are CoI and *sinc* filters.

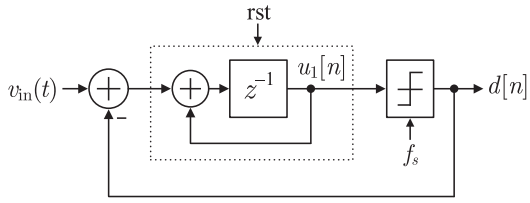

Fig. 2. Generic model of a first-order incremental $\Delta\Sigma$ modulator with a delaying integrator and a one-bit quantizer.

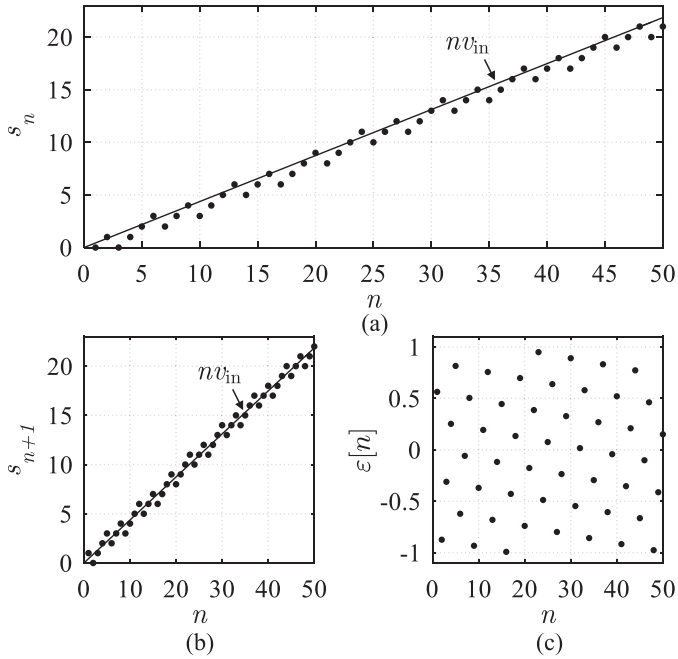

Fig. 3. (a) Lattice diagram depicting the IDC operation (with an example $v_{\text{in}} = +0.437$ and $N = 50$); (b) relative location of the ramp $n \cdot v_{\text{in}}$ and s_{n+1}; and (c) cycle-by-cycle tracking error (quantization error) $\varepsilon[n]$.

III. Proposed L_2MIN^2 Reconstruction Filter

A. Filter Kernel Derivation

As described above, mathematically, the discrete outputs (n, s_{n+1}) track the input ramp (n, nv_{in}) during modulation. If (n, s_{n+1}) are known (i.e., reproduced using the modulator output), we can estimate the input v_{in} by minimizing the MSE between the tracking envelope and the input ramp. We thus use linear least squares regression to minimize the cost function

$$\xi = \frac{1}{2} \sum_{n=1}^{N} (s_{n+1} - n \cdot v_{\text{in}})^2 \tag{4}$$

with respect to v_{in}. ξ is a convex quadratic function, and its minimum can be obtained by

$$\begin{aligned} \frac{\partial \xi}{\partial v_{\text{in}}} &= \sum_{n=1}^{N} (s_{n+1} - n \cdot v_{\text{in}}) \cdot n \\ &= \sum_{n=1}^{N} (n \cdot s_{n+1}) - \sum_{n=1}^{N} (n^2 \cdot v_{\text{in}}) \overset{!}{=} 0 \end{aligned} \tag{5}$$

From this, we obtain the following input estimation $\widehat{v}_{\text{in}}$ after substituting s_{n+1} and $d[0]=0$ to (5).

$$\widehat{v}_{\text{in}}=\sum_{n=1}^{N} n s_{n+1}\Big/\sum_{n=1}^{N} n^2=\sum_{n=1}^{N}\left(n\sum_{i=1}^{n} d[i]\right)\Big/\sum_{n=1}^{N} n^2 \tag{6}$$

To derive the co-factor/weight w_n for each modulator output bit $d[n]$, we regroup the numerator of (6), by observing that

$$\begin{aligned}\sum_{n=1}^{N}\left(n\sum_{i=1}^{n} d[i]\right) &= 1d[1]+\\ &\quad 2d[1]+2d[2]+\\ &\quad 3d[1]+3d[2]+3d[3]+\\ &\quad \vdots\\ &\quad Nd[1]+Nd[2]+Nd[3]+\ldots+Nd[N]\\ &= d[1]\sum_{i=1}^{N} i + d[2]\sum_{i=2}^{N} i + d[3]\sum_{i=3}^{N} +\ldots\\ &= \sum_{n=1}^{N}\left(d[n]\sum_{i=n}^{N} i\right)\end{aligned} \tag{7}$$

From (6) and (7),

$$\widehat{v}_{\text{in}}=\sum_{n=1}^{N}\left(d[n]\underbrace{\sum_{i=n}^{N} i}_{w_n}\right)\Big/\sum_{n=1}^{N} n^2 \tag{8}$$

Therefore, the weight w_n of the n^{th} digital bit $d[n]$ used for input reconstruction is

$$w_n=\sum_{i=n}^{N} i=\sum_{i=1}^{N} i-\sum_{i=1}^{n-1} i=\frac{N(N+1)}{2}-\frac{(n-1)n}{2} \tag{9}$$

The complete reconstruction filter, given by the normalized weighting function $w_n/\sum w_n$, has a concavely smooth-decaying shape. We call this filter L_2min^2 because it is derived by minimizing an L_2-norm, and its weights have a second-order dependency on the bit index n. Fig. 4 shows the normalized weighting function, together with the CoI filters consisting of one and two integrators (i.e., CoI^1, CoI^2) for comparison.

Higher-order IDCs can be analyzed in the same fashion to obtain their L_2-optimal filters. For a given modulator, we derive the time-domain expression of its quantizer input, which can be used to formulate the cost function similar to (4) to obtain the corresponding filter weights. The filter weight of high-order IDC will have a high-order dependency on the bit index. For example, the L_2-optimal filter of a generic second-order modulator is $w_n=\sum_{i=2}^{N-n+1}[i(i+n-1)(i+n-2)]$, which is costly to be implemented in digital circuits. Therefore, in this paper, we just focus on analyzing the performance of the L_2min^2 filter expressed in (9). Meanwhile, only the generic modulator topologies are presented for conciseness, but the proposed filters are applicable to other modulator topologies/variants such as the cascade of integrators with feed-forward (CIFF) architecture, modulator with finite impulse response (FIR) feedback, modulator with signal scaling, etc.

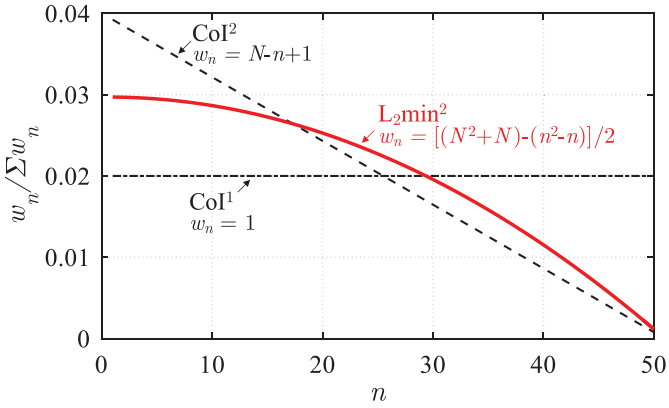

Fig. 4. Normalized weighting function (impulse response) of the proposed L_2min^2 filter and the popular CoI filters, with $N=50$ as an example.

B. Quantization Noise Suppression Capability of L_2min^2

To start, we apply the derived L_2min^2 filter to process the output of a first-order one-bit incremental modulator shown in Fig. 2. For analysis purposes only, assuming infinite operation like a typical $\Delta\Sigma$ modulator [11], its output satisfies

$$d(z)=z^{-1}v_{\text{in}}+\left(1-z^{-1}\right)\varepsilon(z) \tag{10}$$

where $\varepsilon(z)$ is the z-domain quantization error of the one-bit quantizer within the $\Delta\Sigma$-loop. Assuming a constant v_{in} within one conversion (varying inputs discussed later), the time-domain form of (10) is

$$d[n]=v_{\text{in}}+\left(\varepsilon[n]-\varepsilon[n-1]\right) \tag{11}$$

By applying the derived L_2min^2 filter weights, the reconstructed digital output is

$$D_{\text{o}}=\frac{1}{\sum_{n=1}^{N} w_n}\sum_{n=1}^{N}\left(d[n]\cdot w_n\right) \tag{12}$$

$$=v_{\text{in}}+\frac{6}{N(N+1)(2N+1)}\sum_{n=1}^{N} n\varepsilon[n] \tag{13}$$

which contains the input and a linear sum of the quantization errors $\varepsilon[n]$. If $\varepsilon=\{\varepsilon[n], n=1,\ldots,N\}$ is independent, zero mean, and uniformly distributed between ±1 during one conversion [11], its variance is $\sigma_\varepsilon^2=4/12$. Therefore, the standard deviation of the quantization error in D_{o} is

$$\sigma_q=\sqrt{\frac{6}{N(N+1)(2N+1)}}\cdot\sigma_\varepsilon\approx\sqrt{\frac{3}{N^3}}\cdot\sigma_\varepsilon \tag{14}$$

Considering only quantization noise, to achieve k-$\text{bit}_{\text{p-p}}$ (peak-to-peak) resolution within the stable input range $\pm U_{\max}$, the required conversion cycle N using the L_2min^2 filter can be derived with the 3-sigma rule[2] such that

$$3\sigma_q=\frac{\text{LSB}}{2}=\frac{1}{2}\cdot\frac{2U_{\max}}{2^k} \tag{15}$$

[2]some apply a 3.3-sigma rule for peak-to-peak resolution calculation; 1-sigma rule is used to calculate the SQNR.

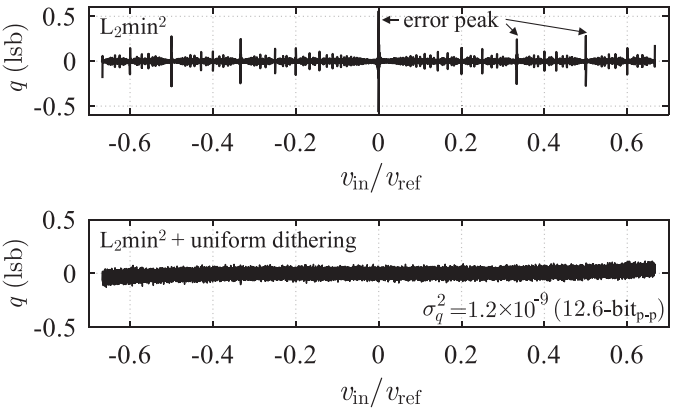

Fig. 5. Quantization error q of different constant v_{in} after being reconstructed by $L_2\text{min}^2$ (one-bit first-order modulator, $N = 1024$, q normalized to 10-bit lsb with $U_{\max} = 2/3$, integrator gain set to 0.75).

From (14) and (15),

$$N = \left(3 \cdot 2^k / U_{\max}\right)^{2/3} \tag{16}$$

Therefore, for IDCs with a target resolution $k > 4$, using $L_2\text{min}^2$ requires much fewer clock cycles compared to using a digital counter for output reconstruction, i.e., $2^k/U_{\max}$ cycles, indicating its strong quantization noise suppression capability.

Due to the inherent non-uniform code length of a first-order modulator [30], it has several *dead zone* regions with large quantization error peaks limiting the absolute conversion precision. These error spikes cannot be mitigated using a multi-level quantizer or an ideal reconstruction filter [19]. Injecting a random dither signal (e.g., uniform dither, Gaussian dither) before the quantizer can address this issue [11], [32]. Dithering can also make ε close to a uniform distribution for DC or slowly time-varying inputs, thus keeping the above-made assumption about ε valid. If a uniform dither signal $\mathcal{U}[-1/3, 1/3]$ is added to the quantizer, σ_ε^2 increases to $(4 + 2/3)/12$ and the allowed input range $U_{\max}$ reduces to about 2/3 to avoid quantizer overloading. To achieve k-bit$_{\text{p-p}}$ resolution, (16) is modified to

$$N_{\text{uniform\_dither}} = 2.2 \cdot \left(2^k / U_{\max}\right)^{2/3} \tag{17}$$

As shown in Fig. 5, the quantization error peaks are successfully mitigated by dithering. The analytical derivation (17) agrees well with the numerical simulation, e.g., 12.6-bit peak-to-peak resolution $log_2\left[U_{\max}/(3 \cdot \sigma_q)\right]$ is achieved with $N = 1024$ and $U_{\max} = 2/3$. The achievable k and crest-factor corrected SQNR at different OSR are shown in Fig. 6, together with that of using CoI^1 and CoI^2 as a performance benchmark[3].

Without loss of generality, $L_2\text{min}^2$ is applicable for varying inputs. With an OSR of 1024 as an example, Fig. 7 presents the simulated output power spectral density (PSD) of a -3.5 dBFS (i.e., $v_{\text{in}} = 2/3$) sinusoidal input after reconstruction by $L_2\text{min}^2$, and the SQNR as a function of the sine-wave amplitude for a generic first-order incremental $\Delta\Sigma$ modulator with uniform dithering. The achieved ~83 dB peak SQNR agrees with our analytical estimation of $20 \cdot log_{10}\left(v_{\text{in}}/\sqrt{2}/\sigma_q\right)$, with σ_q expressed in (14).

[3]consider CoI filter with the same and higher-by-one order of the modulator.

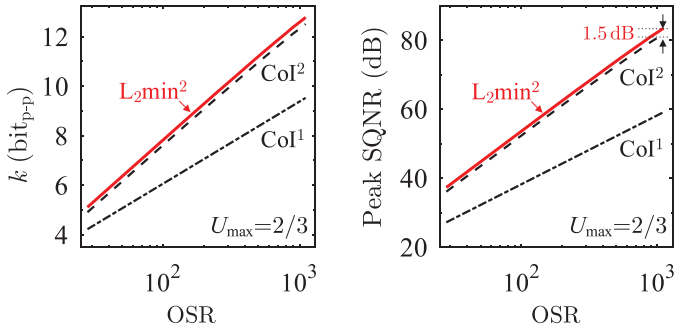

Fig. 6. Considering only quantization noise: peak-to-peak resolution (left) and crest-factor corrected SQNR (right) of the one-bit first-order IDC at different OSR (uniform dithering added excepted when using CoI^1).

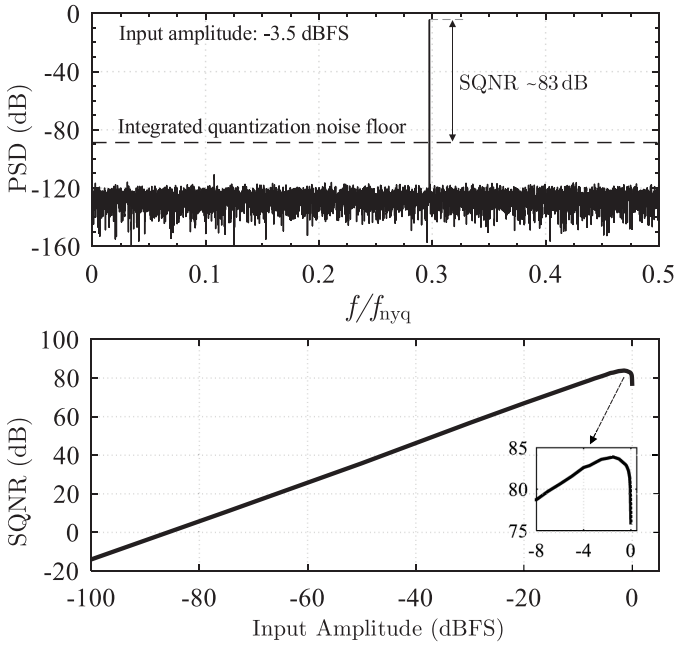

Fig. 7. Simulated power spectral density of a -3.5 dBFS sinusoidal input (top) and SQNR versus the sine-wave input amplitude (bottom), after reconstruction using $L_2\text{min}^2$. Note: First-order incremental $\Delta\Sigma$ modulator with a uniform dithering $\mathcal{U}[-1/3, 1/3]$, $f_{\text{in}} = 594.97$ Hz, $f_s = 2.048$ MHz, $N = 1024$, Nyquist rate $f_{\text{nyq}} = f_s/2/N = 2$ kHz.

C. Thermal Noise Suppression Capability of L_2min^2

In a practical $\Delta\Sigma$ modulator, an unbiased noise component would effectively add to the input, such as the thermal noise with a variance of σ_g^2. A moving averaging filter can effectively suppress the noise to σ_g^2/N after averaging N samples. Any other filter with non-uniform filter weights cannot achieve this level of noise suppression [12]. Usually, the term thermal noise penalty factor β_t is used to represent the increased noise compared to that of using a simple moving average filter, whose β_t is one [22]. For a linear filter with weighting function $\{w_n\}_{n=1}^N$, its β_t is expressed as

$$\beta_t = \frac{\sum_{n=1}^N w_n^2}{\left(\sum_{n=1}^N w_n\right)^2} \Big/ \frac{1}{N} = N \frac{\sum_{n=1}^N w_n^2}{\left(\sum_{n=1}^N w_n\right)^2} \tag{18}$$

The corresponding β_t for the classical linear filters are well-known. For L_2min^2, it can be calculated via

$$\beta_t = N\left[\frac{6}{N(N+1)(2N+1)}\right]^2 \sum_{n=1}^{N}\left[\frac{N^2+N-n^2+n}{2}\right]^2 = \frac{6}{5}\left(1-\frac{N}{2N^2+3N+1}\right) < 1.2 \tag{19}$$

Therefore, the equivalent input-referred noise (IRN) of an IDC after being filtered by L_2min^2 is

$$\sigma^2_{\text{IRN}} < 1.2 \cdot \sigma_g^2/N \tag{20}$$

which is lower than that of using a CoI^2 (i.e., $\beta_t = 1.33$). In other words, without any circuit or system modifications, to achieve the same output thermal noise level, using L_2min^2 can directly reduce 11% of IDC energy consumption compared to that of using a CoI^2. This is the second advantage of L_2min^2 besides its good quantization noise suppression capability, especially when applied to thermal-noise-limited converters.

To summarize, for first-order IDC output reconstruction, L_2min^2 outperforms both in quantization and/or thermal noise suppression compared to the popular CoI^1 and CoI^2 filters. For second-order IDC (listed in Appendix B, Table II), L_2min^2 achieves a comparable quantization noise suppression as that of CoI^2 and CoI^3 but excels for its lower β_t.

IV. Proposed L_2MIN^{2s} Reconstruction Filter

Despite the advantages of L_2min^2, it has the shortcoming of being unable to reject periodic noise (e.g., line frequency disturbance) due to its asymmetric weighting function. The existing popular IDC reconstruction filter with periodic noise rejection capability is the moving average filter, which is also called $sinc^L$ filter with L representing the order [33]. In the following, we present a new filter L_2min^{2s} with efficient quantization noise, thermal noise, and periodic noise suppression.

A. Symmetric Filter Kernel of L_2min^{2s}

Based on the L_2min^2 kernel discussed in Section III, we now develop a filter L_2min^{2s} with a symmetric impulse response. To construct such a new kernel with $2M-1$ points (i.e., an odd number and now the IDC's OSR is $2M-1$), w_n in (9) is firstly left-shifted by 1-point, mirrored around the y-axis, and then right-shifted by M-points, with the analytical form of the symmetric filter expressed as

$$w_n = \begin{cases} \dfrac{M^2+M}{2} - \dfrac{(M-n+1)^2-(M-n+1)}{2} & n = 1,2,\cdots,M \\ \dfrac{M^2+M}{2} - \dfrac{(n-M+1)^2-(n-M+1)}{2} & n = M+1,\cdots,2M-1 \end{cases} \tag{21}$$

where $w_n = 0$ for $n \geqslant 2M$. The normalized weighing function of L_2min^{2s} is shown in Fig. 8, together with the first-order (same as CoI^1), second-order, and third-order *sinc* filters for direct comparison. The thermal noise penalty β_t of L_2min^{2s} is still 1.2, which is smaller than that of the $sinc^2$ (i.e., 1.33) and $sinc^3$ (i.e., 1.67). This is the first advantage of L_2min^{2s}.

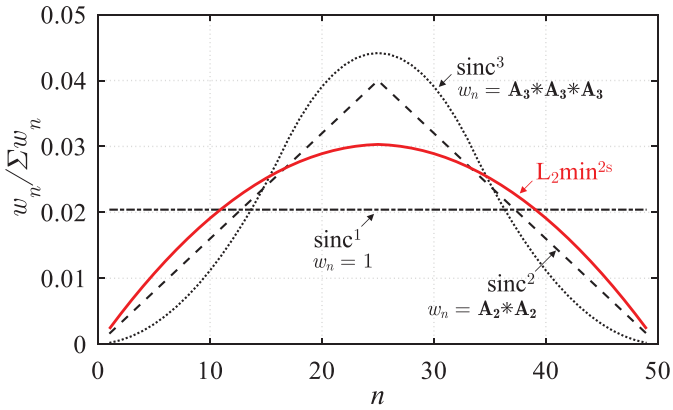

Fig. 8. Normalized weighting function of the first, second, third-order *sinc* filter and the L_2min^{2s} filter (a length of 49-point as an example, $\mathbf{A}_2$ is a 25-element row vector $[1,1,\cdots,1]$, $\mathbf{A}_3$ is a 17-element row vector $[1,1,\cdots,1]$, * denotes convolution).

B. Frequency Response of L_2min^{2s}

One of the most important features of a symmetric filter is the number and locations of its frequency notches. For the well-known $sinc^L$ filter, its z-domain transfer function is

$$H(z) = \frac{1}{D^L} \cdot \left(\frac{1-z^{-D}}{1-z^{-1}}\right)^L \tag{22}$$

where D is the filter decimation ratio. It provides frequency notches at the integer multiples of f_s/D, i.e., jf_s/D with $j \in \{1,2,\ldots,D-1\}$ and f_s is the bitstream data rate. The required bitstream length is $D \cdot L - (L-1)$ to produce a valid reconstructed output [34]. Therefore, for a given f_s and D to place the first notch f_s/D at the desired frequency, e.g., 50 Hz or 60 Hz, the IDC conversion speed becomes slower when a higher-order *sinc* filter is adopted. This tradeoff between frequency notch location, stopband attenuation, and conversion speed is a major drawback of *sinc* filters.

For the proposed L_2min^{2s} filter described by (21), its z-domain transfer function is

$$H(z) = \frac{1}{\sum_{n=1}^{2M-1} w_n} \sum_{i=1}^{2M-1} w_i \cdot z^{i-(2M-1)} \tag{23}$$

As detailed in Appendix A, it creates $(2M-2)$ frequency notches between 0 and f_s, with its first notch frequency at about $3/(4M) \cdot f_s$. Fig. 9 shows its frequency response, together with that of the $sinc^{1,2,3}$ filters for comparison. L_2min^{2s} has a moderate roll-off at 40 dB/decade, and its number of frequency notches is 2 and 3 times that of the $sinc^2$ and $sinc^3$ filter with the same kernel length, respectively. This is the second advantage of L_2min^{2s}.

C. Quantization Noise Suppression Capability of L_2min^{2s}

L_2min^{2s} can be applied to reconstruct first-order IDC outputs, and its quantization noise suppression capability outperforms that of the $sinc^1$ and $sinc^2$ filters (listed in Appendix B, Table II). Here we focus on analyzing its performance when applied to the popular second-order IDC with a pure differential noise transfer function [11], as shown in Fig. 10.

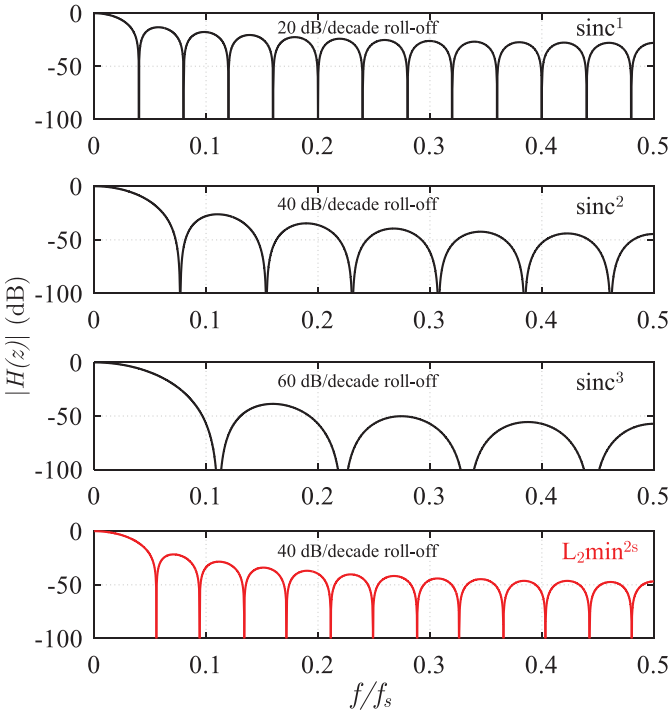

Fig. 9. Frequency response of $sinc^{1,2,3}$ and the L_2min^{2s} filter with a 25-point length ($M = 13$). The filter input data rate is f_s.

Following a similar analysis presented in Section III-B, the second-order IDC output satisfies

$$d_2(z) = z^{-2}v_{\text{in}} + \left(1 - z^{-1}\right)^2 \varepsilon(z) \tag{24}$$

Assuming a constant v_{in}, the time-domain form of (24) is

$$d_2[n] = v_{\text{in}} + (\varepsilon[n] - 2\varepsilon[n-1] + \varepsilon[n-2]) \tag{25}$$

By applying the L_2min^{2s} filter weights, the reconstructed digital output is

$$D_{o2} = \frac{1}{\sum_{n=1}^{2M-1} w_n} \sum_{n=1}^{2M-1} (w_n \cdot d_2[n]) \tag{26}$$

$$= v_{\text{in}} + \frac{6}{M(M+1)(4M-1)} \sum_{n=1}^{2M-1} (w_n \cdot d_2[n]) \tag{27}$$

Similarly, if $\varepsilon = \{\varepsilon[n]\}_{n=1}^{N}$ is independent, uniformly distributed, and has zero mean (the validation of this assumption will be revisited later), the standard deviation of the quantization error in D_{o2} is

$$\sigma_q = \frac{6}{M(4M-1)} \cdot \sigma_\varepsilon \approx \frac{3}{2M^2}\sigma_\varepsilon \tag{28}$$

For a one-bit quantizer with $\sigma_\varepsilon^2 = 4/12$, following the 3-sigma rule, (29) must hold to achieve k-bit resolution (considering only quantization noise) within the stable input range $\pm U_{\max}$,

$$3 \cdot \frac{3}{2M^2} \cdot \frac{2}{\sqrt{12}} = \frac{\text{LSB}}{2} = \frac{1}{2} \cdot \frac{2U_{\max}}{2^k} \tag{29}$$

Therefore,

$$M = \sqrt{3\sqrt{3} \cdot 2^{(k-1)}/U_{\max}} \tag{30}$$

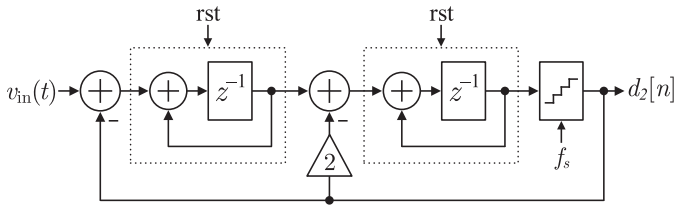

Fig. 10. Generic model of a second-order incremental $\Delta\Sigma$ modulator with delaying integrators.

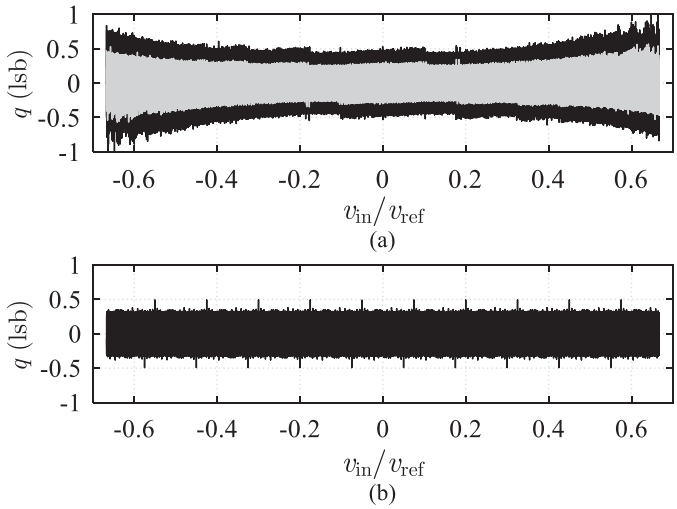

Fig. 11. (a) Quantization error q of a one-bit second-order modulator reconstructed by L_2min^{2s} at OSR = 1000. The light-color curve is at OSR = 1300 after correcting (30) using a 5-sigma rule; (b) Quantization error of a multi-bit ($l = 17$) second-order incremental $\Delta\Sigma$ modulator reconstructed by L_2min^{2s} at OSR = 250. q is normalized to 16-bit lsb with $U_{\max} = 2/3$.

Similarly, for modulator using an l-level multi-bit quantizer, we have $\sigma_\varepsilon^2 = 4/\left[12 \cdot (l-1)^2\right]$, thus

$$M = \sqrt{3\sqrt{3} \cdot 2^{(k-1)}/U_{\max}/(l-1)} \tag{31}$$

It is worth repeating that the total number of required conversion cycles and the filter length is $(2M-1)$. For example, with $l = 2$ and $U_{\max} = 2/3$, it requires about 1000 cycles to achieve 16-bit resolution using L_2min^{2s} to reconstruct the second-order IDC output.

1) Numerical Verification: To verify our analysis, an input sweep between $\pm U_{\max}$ is applied to the modulator in Fig. 10. The quantization errors after being filtered by L_2min^{2s} are shown in Fig. 11. With a one-bit quantizer, the quantization error is greater than the allowed 0.5 LSB when the inputs are close to $\pm U_{\max}$. It means the required conversion cycle is underestimated by (30). The main reason is that ε becomes highly correlated at larger v_{in}. By applying a 5-sigma rule, (30) can be corrected to match with the simulation results (i.e., change $3\sqrt{3}$ in (30) to $5\sqrt{3}$). With a multi-bit quantizer, the assumptions about ε hold and the numerical results agree well with the estimation by (31) (slightly conservative), and the worst-case errors are below 0.5 LSB. The quantization error peaks shown in the plots will disappear in actual implementations, with the circuit noise performing as an effective dithering signal.

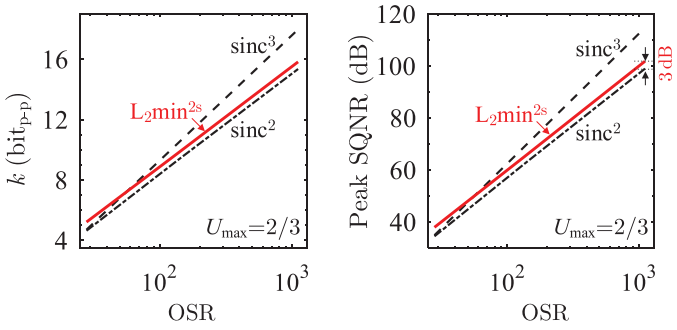

Fig. 12. Considering only quantization noise: peak-to-peak resolution (left) and crest-factor corrected SQNR (right) of the one-bit second-order IDC at different OSRs.

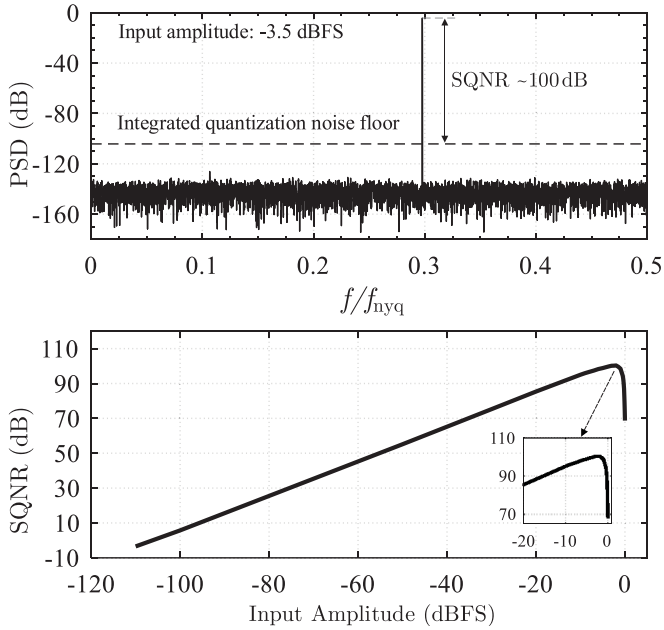

Fig. 13. Simulated power spectral density of a -3.5 dBFS sinusoidal input (top) and SQNR versus the sine-wave input amplitude (bottom), after reconstruction using $\mathrm{L_2min}^{2s}$. Note: Second-order incremental $\Delta\Sigma$ modulator, $f_{\mathrm{in}} = 594.97$ Hz, $f_s = 2.048$ MHz, $M = 512$, Nyquist rate $f_{\mathrm{nyq}} = f_s/2/(2M-1) = 2$ kHz.

Using a one-bit second-order IDC as an example, the achievable k and crest-factor corrected SQNR using $\mathrm{L_2min}^{2s}$ is shown in Fig. 12, together with that of *sinc*^{2} and *sinc*^{3} for comparison[4]. Although the quantization noise suppression capability of *sinc*^{3} is slightly better than that of $\mathrm{L_2min}^{2s}$, its high β_t of 1.67 is a significant drawback. Practically, various techniques can be used together with the filter to suppress quantization noise. Thus, most high-resolution IDCs are designed to be thermal-noise-limited [1]. Therefore, owing to its good quantization noise suppression and low β_t, $\mathrm{L_2min}^{2s}$ is an excellent option for second-order IDC output reconstruction when periodic noise suppression is mandatory, where *sinc*^{2} and *sinc*^{3} filters are usually employed. This is the third advantage of $\mathrm{L_2min}^{2s}$.

Without loss of generality, Fig. 13 presents the simulation results using $\mathrm{L_2min}^{2s}$ for varying inputs with an OSR of 1024

[4]consider *sinc* filter with the same and higher-by-one order of the modulator.

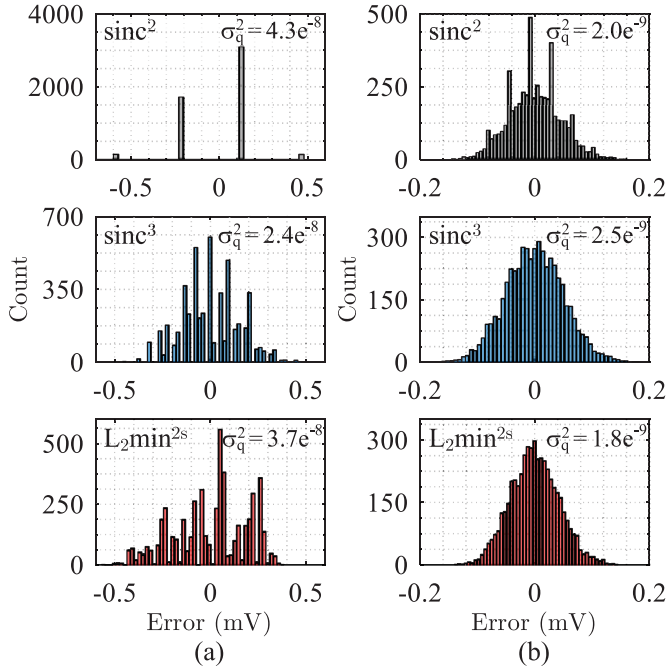

Fig. 14. Measured second-order IDC output error reconstructed by different linear filters; (a) at a low OSR when quantization noise dominates; and (b) at a high OSR when thermal noise dominates.

as an example. It shows the output power spectral density of a -3.5 dBFS sinusoidal input and the SQNR as a function of the sine-wave amplitude after reconstruction by $\mathrm{L_2min}^{2s}$ for a generic second-order incremental $\Delta\Sigma$ modulator. The achieved $\sim$100 dB peak SQNR also agrees with our analytical estimation of $20 \cdot log_{10}\left(v_{\mathrm{in}}/\sqrt{2}/\sigma_q\right)$, with σ_q defined in (28).

2) Experimental Verification: We verified the performance of $\mathrm{L_2min}^{2s}$ by using it to reconstruct the output of a second-order IDC chip prototype designed in [29]. As shown in Fig. 14, $\mathrm{L_2min}^{2s}$ outperforms *sinc*^{2} at a low OSR when quantization noise dominates, and it outperforms both *sinc*^{2} and *sinc*^{3} at a high OSR when thermal noise dominates, which agrees with the analysis above. Specifically, to achieve the same output thermal noise level, the IDC can save approximately 28% of energy when using $\mathrm{L_2min}^{2s}$ instead of *sinc*^{3} for output reconstruction.

To summarize, when periodic noise suppression is necessary, owing to the low thermal noise penalty, more frequency notches, and strong quantization noise suppression capability, the symmetric $\mathrm{L_2min}^{2s}$ filter excels for both first-order and second-order IDC output reconstruction, especially for high-resolution thermal-noise-limited ones.

V. Design Example Using the Proposed Filters

As analyzed above, using different filters for IDC output reconstruction can significantly affect its performance. The proposed $\mathrm{L_2min}^2$ filter and its symmetric version $\mathrm{L_2min}^{2s}$ exhibit both good thermal noise and quantization suppression properties and are excellent candidates for first-order and second-order IDC output reconstruction. The flow of designing an IDC using the proposed filters is straightforward. For example, to achieve 17-bit peak-to-peak thermal-noise-limited resolution for an input range of ± 0.6 V with a 1.2 V reference voltage, a sampling

clock frequency f_s of 40 kHz, and a periodic frequency noise at 50 Hz (i.e., $1/800 \cdot f_s$), the design proceeds as follows.

1) *Noise distribution:* achieving 17-bit within ±0.6 V means one LSB is $2 \cdot 0.6/2^{17} = 9.2\,\mu$V. For peak-to-peak resolution, by applying a 3-sigma rule, the total allowable noise standard deviation is $9.2\,\mu\text{V}/2/3 = 1.6\,\mu$V. Thus, the total noise power in the reconstructed output is $\sigma_o^2 = 2.56\,\text{pV}^2$. If quantization noise contributes 20% of the total noise with 80% being thermal noise, the allowed quantization noise power is $\sigma_q^2 = 0.5\,\text{pV}^2$. This is equivalent to achieving a 18.1-bit quantization-noise-only resolution within ±0.6 V (the normalized $U_{\max}$ is 0.6 V/1.2 V = 0.5).
2) *Number of conversion cycles:* a multi-bit second-order modulator is used for such a high-resolution IDC. Considering the requirement of periodic noise suppression, we will use $L_2\text{min}^{2s}$. In this example, we choose $l = 9$ considering the DAC implementation and matching complexity. From Table II in Appendix B, the required number of conversion cycles is $3.2 \cdot (2^{18.1}/0.5/8)^{1/2} = 848$.
3) *Periodic noise suppression:* we place the first notch $3/(4M) \cdot f_s$ of $L_2\text{min}^{2s}$ at 50 Hz, thus M should be 600. The total number of conversion cycles is 1200, which is enough for quantization noise suppression as calculated above. Next, we can verify the exact zero locations using Matlab (see Appendix A) and fine-tune the conversion cycles. From the numerical verification, an OSR of 1145 can best suppress the line noise.
4) *Thermal noise design:* after knowing the thermal noise budget ($= 0.8 \cdot 2.56\,\text{pV}^2$), the total conversion cycles, and considering the filter's thermal noise penalty (i.e., 1.2), the IDC's input-referred thermal noise budget is $\sigma_{\text{IRN}}^2 = 2.06\,\text{pV}^2 \cdot 1145/1.2 \approx 2\,\text{nV}^2$. The modulator can then be designed after a system-level verification, e.g., using our open-source modulator simulation script.

VI. Digital Implementation

The proposed linear filters are hardware-friendly to be implemented on-chip. In this section, we present two examples to design the $L_2\text{min}^2$ and $L_2\text{min}^{2s}$ filter for one-bit input. FPGA and ASIC implementation results will also be discussed. Other implementations will also work if the filter kernel function (9) or (21) is satisfied.

A. Implementation of L_2min^2

An example realization of the N-point filter weighting function (9) for $L_2\text{min}^2$ with one-bit input is shown in Fig. 15. It requires a ripple counter, a subtractor, an adder, and an AND-gate. Initially, the ripple counter is reset to 0, while the subtractor is reset to $w_N = N(N+1)/2$. The weight generator updates its output w_n at f_s (the input data rate). The adder is gated by $d[n]$ and is updated only when the input bit is "1". Notice that the adder operates at the falling edge of f_s thus preparing the correct weight w_n.

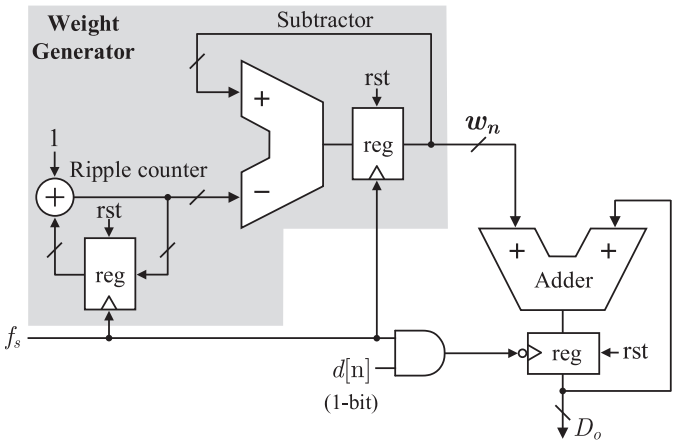

Fig. 15. Example implementation of the $L_2\text{min}^2$ filter with one-bit input.

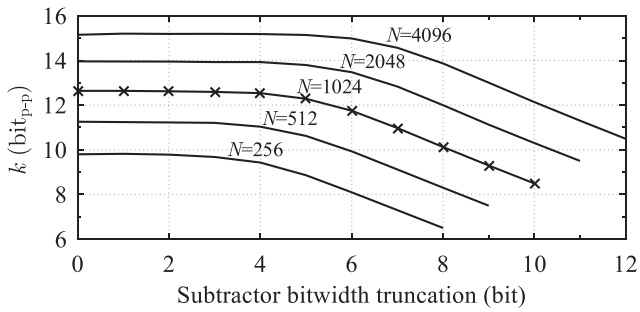

Fig. 16. Achieved first-order IDC resolution after subtractor (and adder) bitwidth truncation, with the same simulation setup as in Fig. 5.

Similar to Hogenauer [20], we use the worst-case register growth to calculate the bitwidth requirement of each building block, which is $\lceil log_2(N+1) \rceil$ for the ripple counter, $\lceil log_2(N^2+N) - 1 \rceil$ for the subtractor, and $(3\lceil log_2 N \rceil - 1)$ for the adder. Practically, truncation can be applied to the subtractor and adder to reduce the number of registers (i.e., truncating w_n). For example, refer to (17), a resolution of 12.6-bit can be achieved with an N of 1024 using $L_2\text{min}^2$ for output reconstruction. Ideally, the ripple counter, subtractor, and adder bitwidths are 11, 20, and 29, respectively. As shown in Fig. 16, the resolution loss is only 0.06-bit after truncating the subtractor and adder by 4 bit (i.e., from 20 to 16 bit). Based on the numerical simulation results, truncating the subtractor bitwidth by 20% of its theoretical value has negligible influences on the IDC performance.

B. Implementation of L_2min^{2s}

The $(2M-1)$-point filter kernel of (21) for $L_2\text{min}^{2s}$ with one-bit input can be implemented by re-using the architecture of Fig. 15, with the modified design shown in Fig. 17. Initially, the ripple counter output is reset (via rst_c) to M and configured as a down counter. The S/A block performs as an adder with its initial output reset to 0. After operating for M clock cycles, the counter output will be 0. Its output is then reset to 1 and configured as an up-counter. The S/A is reconfigured as a subtractor. The filter then operates for another

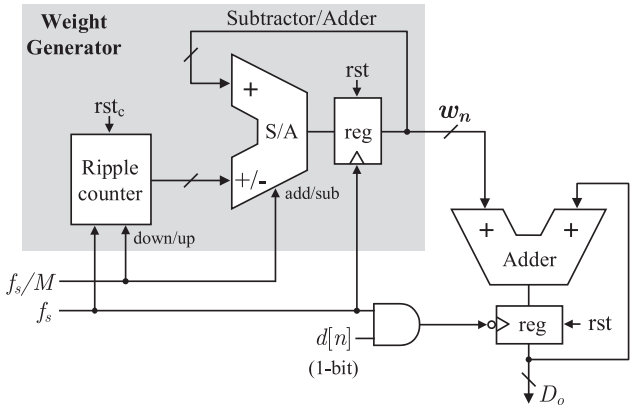

Fig. 17. Example implementation of the L_2min^{2s} filter with one-bit input.

M clock cycle (the last weight $w_{2M} = 0$) to finish one IDC sample reconstruction. Finally, the filter is reset for the next conversion. The required bitwidths for the counter, S/A block, and the adder are $\lceil log_2(M+1) \rceil$, $\lceil log_2\left(M^2+M\right)-1 \rceil$, and $3\lceil log_2 M \rceil$, respectively. Similarly, bit truncation of the S/A and adder block can be applied. The conclusion drawn above still holds that truncating the S/A bitwidth (and thus the adder) by 20% of its theoretical value does not affect the IDC performance.

The above design examples are for one-bit input, for multi-bit $d[n]$ (e.g., B-bit), a $B \times \lceil log_2\left(M^2+M\right)-1 \rceil$ bit multiplier can be used to compute $d[n] \cdot w_n$, whose hardware overhead becomes slightly higher. Efficient implementation of (9) and (21) for multi-bit input deserves further investigation.

C. Synthesis Results

Apart from the fully customized digital design, the proposed linear filters can also be handily synthesized for FPGA and ASIC targets. For instance, the L_2min^2 and L_2min^{2s} filters without register bitwidth truncation are synthesized herein for one-bit input and operate for 1024 cycles. FPGA synthesis was performed using Vivado for an Artix-7 device, xc7a12tcpg238-3. ASIC synthesis was performed using Synopsys design compiler targeting a commercial standard cell library in 180 nm CMOS technology with a 1.8V supply. Running at an example 1 MHz input data rate, the worst-case power dissipation is simulated using the cadence Spectre platform with $d[n] \equiv 1$ (i.e., all bits are one to keep the filter busy, which will not occur in actual conversion unless the modulator and, thus, the quantizer is overloaded; the purpose here is to estimate the upper limit of the filter's power consumption). For performance benchmarks, the synthesis results of L_2min^2 and L_2min^{2s} are shown in Fig. 18, together with the popular high-order CoI and *sinc* filters (using CIC architecture working in one-shot mode, and with a differential delay of one in the comb stage [20]). As expected, CoI^2 occupies a smaller area and consumes less power due to its simple topology. However, it is less used due to its thermal noise penalty and lack of frequency notches. The proposed filters show high area efficiency with comparable power consumption but excel for their low

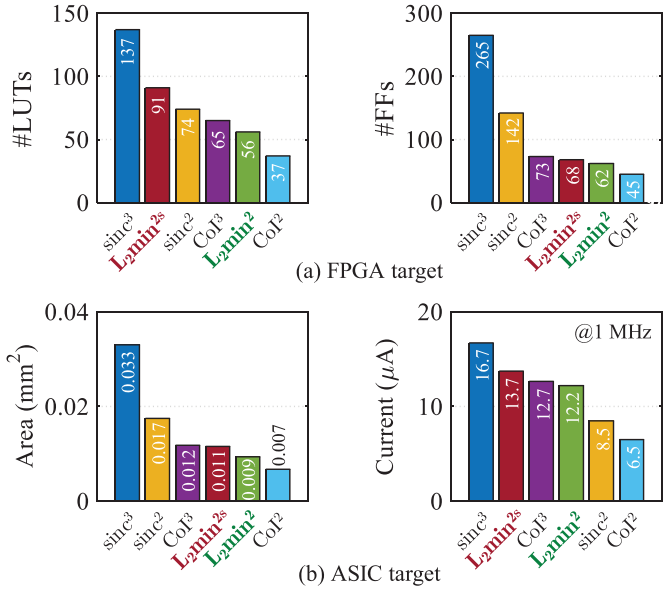

Fig. 18. Hardware complexity of L_2min^2 and L_2min^{2s} implemented in (a) an Artix-7 FPGA and (b) a 180 nm process ASIC target (FPGA power consumption is not shown as the estimation is not accurate for small digital designs. #LUTs: number of the look-up tables, #FF: number of flip-flops).

β_t. In IDC designs, the power and area of the digital filter are often negligible compared to that consumed by the analog integrators.

VII. Summary and Discussion

To summarize, two linear reconstruction filters for IDC are proposed, with analytical, numerical, and experimental results presented to demonstrate their overall superior performance for first-order and second-order incremental $\Delta\Sigma$ modulators in terms of quantization noise suppression, thermal noise suppression, and hardware complexity. Table I also compares other key metrics of the proposed L_2min^{2s} filter, such as the frequency notch, stop-band roll-off, etc., with the popular linear filters. Specifically, the advantages of employing the proposed reconstruction filters include the following. (1) It has a low thermal noise penalty of 1.2, the smallest among the existing high-order linear filters. To achieve the same output thermal noise level after reconstruction, using $L_2min^{2/2s}$ can reduce the IDC energy consumption by 11%, 28%, and 33% compared to that of using a CoI^2/*sinc*^{2}, *sinc*^{3}, and CoI^3 filter, respectively. (2) In addition, when periodic noise suppression is needed, the L_2min^{2s} filter can provide more frequency notches than other high-order *sinc* filters, thus suppressing periodic noise (e.g., designing the first notch of the filter to be the same as the periodic noise frequency) without greatly sacrificing the IDC's sampling rate. For example, at an OSR of 512, compared to the Steensgaard's approach [22], the L_2min^{2s} filter can achieve about 40 dB higher SNR when applied to a generic second-order modulator. In this paper, for conciseness, only the generic modulator topologies are analyzed in detail, but the proposed filters are applicable to other modulator topologies/variants as indicated in Appendix B, Table II, and

TABLE I
PERFORMANCE SUMMARY OF DIFFERENT LINEAR RECONSTRUCTION FILTERS FOR IDCs

Filter with $(2M-1)^\flat$ points	**CoI^2**	**CoI^3**	**L$_2$min^2**	**sinc^1**	**sinc^2**	**sinc^3**	**L$_2$min^{2s}**
Noise penalty β_t	1.33	1.8	**1.2**	1	1.33	1.67	**1.2**
With frequency notches	No	No	**No**	Yes	Yes	Yes	**Yes**
Number of notches$^\sharp$	0	0	**0**	$2M-2$	$(2M-2)/2$	$(2M-2)/3$	$\boldsymbol{2M-2}$
First notch frequency	n/a	n/a	**n/a**	$f_s/(2M-1)$	f_s/M	$3f_s/(2M+1)$	$\boldsymbol{\sim 3f_s/(4M)}$
Roll-off (dB/decade)	20	20	**20**	20	40	60	**40**

$^\flat$An odd number and with $(2M-2)$ divisible by 3. $^\sharp$Between 0 and the input data rate f_s.

can be verified using our open-source numerical simulation scripts.

VIII. CONCLUSION

Two efficient linear reconstruction filters, L$_2$min^2 and L$_2$min^{2s}, are presented in this article. The filter kernel is derived based on the L$_2$-norm to achieve a globally minimized IDC output reconstruction error. It exhibits the lowest thermal noise penalty compared with the classical high-order linear filters while providing a strong quantization noise suppression capability. Implementation of the filters is hardware friendly. Overall, L$_2$min^2 and L$_2$min^{2s} are excellent candidates for first- and second-order modulator output reconstruction, especially for thermal-noise-limited ones. Methodologies presented in this paper can also be used to derive filters for higher-order IDCs. Some efforts are still required to extend our method, including implementing the proposed linear filters for multi-bit inputs with minimal hardware resources and extending the filter implementation for free-running $\Delta\Sigma$ ADCs.

APPENDIX A

This appendix provides the derivation of the number and location of the zeros in the transfer function of the proposed L$_2$min^{2s} filter. For a $(2M-1)$-point symmetric filter described by (21), its z-domain transfer function is (without including the filter normalization term $1/\sum_{n=1}^{2M-1} w_n$)

$$H(z) = \sum_{i=1}^{2M-1} w_i z^{i-(2M-1)} \tag{a1}$$

Therefore,

$$z^{-1}H(z) = \sum_{i=1}^{2M-1} w_i z^{i-2M} \tag{a2}$$

and

$$\begin{aligned} H(z) - z^{-1}H(z) &= \sum_{i=1}^{2M-1} w_i z^{i-(2M-1)} - \sum_{i=1}^{2M-1} w_i z^{i-2M} \\ &= \sum_{i=0}^{2M-1} (w_i - w_{i+1}) z^{i-(2M-1)} \\ &= \sum_{i=1}^{M} (M+1-i) z^{1-i} - \sum_{i=1}^{M} i z^{1-i-M} \end{aligned} \tag{a3}$$

Multiplying both sides by z^{-1} yields

$$\begin{aligned} z^{-1}\left[H(z) - z^{-1}H(z)\right] &= \sum_{i=1}^{M} (M+1-i) z^{-i} \\ &\quad - \sum_{i=1}^{M} i z^{-i-M} \end{aligned} \tag{a4}$$

By subtracting (a4) from (a3), we obtain

$$\begin{aligned} \left(1-z^{-1}\right)^2 H(z) &= M - \sum_{i=1}^{M} z^{-i} + Mz^{-2M} - \sum_{i=1}^{M} z^{-i-M+1} \\ &= M - \frac{z^{-1}\left(1-z^{-M}\right)}{1-z^{-1}} \\ &\quad + Mz^{-2M} - \frac{z^{-M}\left(1-z^{-M}\right)}{1-z^{-1}} \end{aligned} \tag{a5}$$

Finally,

$$\begin{aligned} H(z) = \frac{1}{\left(1-z^{-1}\right)^3} \Big[& M - (M+1) z^{-1} \\ & - z^{-M} + z^{-(M+1)} \\ & + (M+1) z^{-2M} - M z^{-(2M+1)} \Big] \end{aligned} \tag{a6}$$

From (a6), $H(z)$ has three poles at $z=1$ (i.e., $f=0$) of the z-plane. Its zeros are the roots of $H(z)=0$, with

$$\begin{aligned} & Mz^{(2M+1)} - (M+1) z^{2M} - z^{M+1} \\ & \quad + z^M + (M+1)z - M = 0 \end{aligned} \tag{a7}$$

According to the fundamental theorem of algebra, (a7) has $(2M+1)$ roots, meaning (a6) provides $(2M+1)$ zeros in the frequency domain. Assuming M is large and $M+1 \approx M$ holds, (a7) is modified to

$$\begin{aligned} & Mz^{(2M+1)} - Mz^{2M} - z^{M+1} + z^M + Mz - M \\ & \quad = M(z-1)\left(z^{2M} - 1/M \cdot z^M + 1\right) = 0 \end{aligned} \tag{a8}$$

The first root of (a8) is

$$z = 1 \tag{a9}$$

and the rest $2M$ roots are

$$z = \left(\frac{1}{2M} \pm j\sqrt{1 - \frac{1}{4M^2}}\right)^{1/M} \tag{a10}$$

TABLE II
NUMBER OF CYCLES (OSR) TO ACHIEVE k-BIT PEAK-TO-PEAK RESOLUTION WITHIN $U^*_{\max}$ FOR DIFFERENT MODULATOR TOPOLOGY AND RECONSTRUCTION FILTER COMBINATIONS

		One-bit mod1†	One-bit mod2$^\sharp$	Multi-bit mod2$^\flat$
Without periodic noise suppression	**CoI**^{2}	$2.4\cdot\left(2^k/U_{\max}\right)^{2/3}$	$2.5\cdot\left(2^k/U_{\max}\right)^{1/2}$	$1.9\cdot\left[2^k/U_{\max}/\left(l-1\right)\right]^{1/2}$
	CoI^3	not preferred	$2.5\cdot\left(2^k/U_{\max}\right)^{1/2\star}$	$2.6\cdot\left[2^k/U_{\max}/\left(l-1\right)\right]^{2/5}$
	L$_2$min^2	$2.2\cdot\left(2^k/U_{\max}\right)^{2/3}$	$3.0\cdot\left(2^k/U_{\max}\right)^{1/2}$	$2.3\cdot\left[2^k/U_{\max}/\left(l-1\right)\right]^{1/2}$
With periodic noise suppression	**sinc**^{1}	$2^k/U_{\max}$	not preferred	not preferred
	sinc^2	$3.8\cdot\left(2^k/U_{\max}\right)^{2/3}$	$5.0\cdot\left(2^k/U_{\max}\right)^{1/2}$	$3.9\cdot\left[2^k/U_{\max}/\left(l-1\right)\right]^{1/2}$
	sinc^3	not preferred	$8.2\cdot\left(2^k/U_{\max}\right)^{2/5}$	$6.7\cdot\left[2^k/U_{\max}/\left(l-1\right)\right]^{2/5}$
	L$_2$min^{2s}	$3.5\cdot\left(2^k/U_{\max}\right)^{2/3}$	$4.1\cdot\left(2^k/U_{\max}\right)^{1/2}$	$3.2\cdot\left[2^k/U_{\max}/\left(l-1\right)\right]^{1/2}$

$^*U_{\max}$ is the normalized input range w.r.t. its reference and is a dimensionless number.
†Except for sinc^1, the rest are derived under a uniform dithering of $U\{-1/3, 1/3\}$ with $U_{\max}\leqslant 2/3$.
$^\sharp$5-sigma rule applied as explained in Section III-C, with $U_{\max}\leqslant 2/3$.
*Fitted expression, same performance as CoI^2 due to the large nonlinearity after reconstruction.
$^\flat$Derivations are valid for $l\geqslant 9$ with $U_{\max}\leqslant 2/3$ (if a 2-bit quantizer with $l=5$ is used, $U_{\max}\leqslant 1/2$).

which are all on the unit circle of the z-plane (i.e., $|z|=1$). By applying Euler's formula to (a10), we arrive at

$$z = exp\left[\pm j\left(\arccos\frac{1}{2M}+2\pi k\right)\right]^{1/M} \quad k=0,1,\cdots,M-1 \tag{a11}$$

Therefore, besides the zero at $f=0$ indicated by (a9), two more zeros at $f=0$ will be produced as in (a11) (following the assumption of a large M). Therefore, the three zeros and three poles cancel and $|H(1)|=1$ holds after normalization (i.e., no DC signal attenuation). The frequencies of the other $(2M-2)$ zeros indicated by (a11) are at

$$f=\left[\frac{\arccos\left(1/\left(2M\right)\right)}{2\pi M}+\frac{k}{M}\right]f_s\approx\left[\frac{1+4k}{4M}\right]f_s \quad k=1,2,\cdots,M-1 \tag{a12}$$

and

$$f=\left[1-\frac{\arccos\left(1/\left(2M\right)\right)}{2\pi M}-\frac{k}{M}\right]f_s\approx\left[1-\frac{1+4k}{4M}\right]f_s \quad k=M-1,\cdots,2,1 \tag{a13}$$

where f_s is the filter input data rate. The frequency of the first zero can be found by (a13) with $k=(M-1)$, which is $3/\left(4M\right)\cdot f_s$. Note that (a12) and (a13) are close estimations of the zero locations. After deriving the weighting function w_n as described in Section IV-A, the provided Matlab script[5] can be utilized to produce the pole-zero plots and frequency response during design, thus finding the exact zero frequencies of the filter.

APPENDIX B

For clarity, analysis of the L$_2$min^2 filter applied to a second-order modulator and the L$_2$min^{2s} filter applied to a first-order modulator is not included in the body of the paper, which can be derived following the same procedures presented in Sections III-B and IV-C, respectively. In this appendix, we derive and tabulate the number of clock cycles (i.e., OSR) required to achieve k-bit peak-to-peak resolution within $U_{\max}$ (considering only quantization noise) for the popular one-bit first-order, one-bit second-order, and multi-bit second-order incremental $\Delta\Sigma$ modulators reconstructed by different linear filters. The analytical expressions in Table II agree well with the numerical simulations and can be utilized for theoretical calculation during design. The analytical expressions hold for both constant and varying input signals. Practically, changes in modulator parameters can cause a difference. System-level simulations or experimental measurements should be used to verify the calculated OSR during design.

[5]download from github.com/bowanghbku/L2min2-Filter/

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This article has supplementary downloadable material available at github.com/bowanghbku/L2min2-Filter, provided by the author. The material includes the Matlab simulation and Verilog implementation code.

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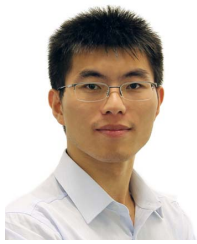

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